

FIG. 1

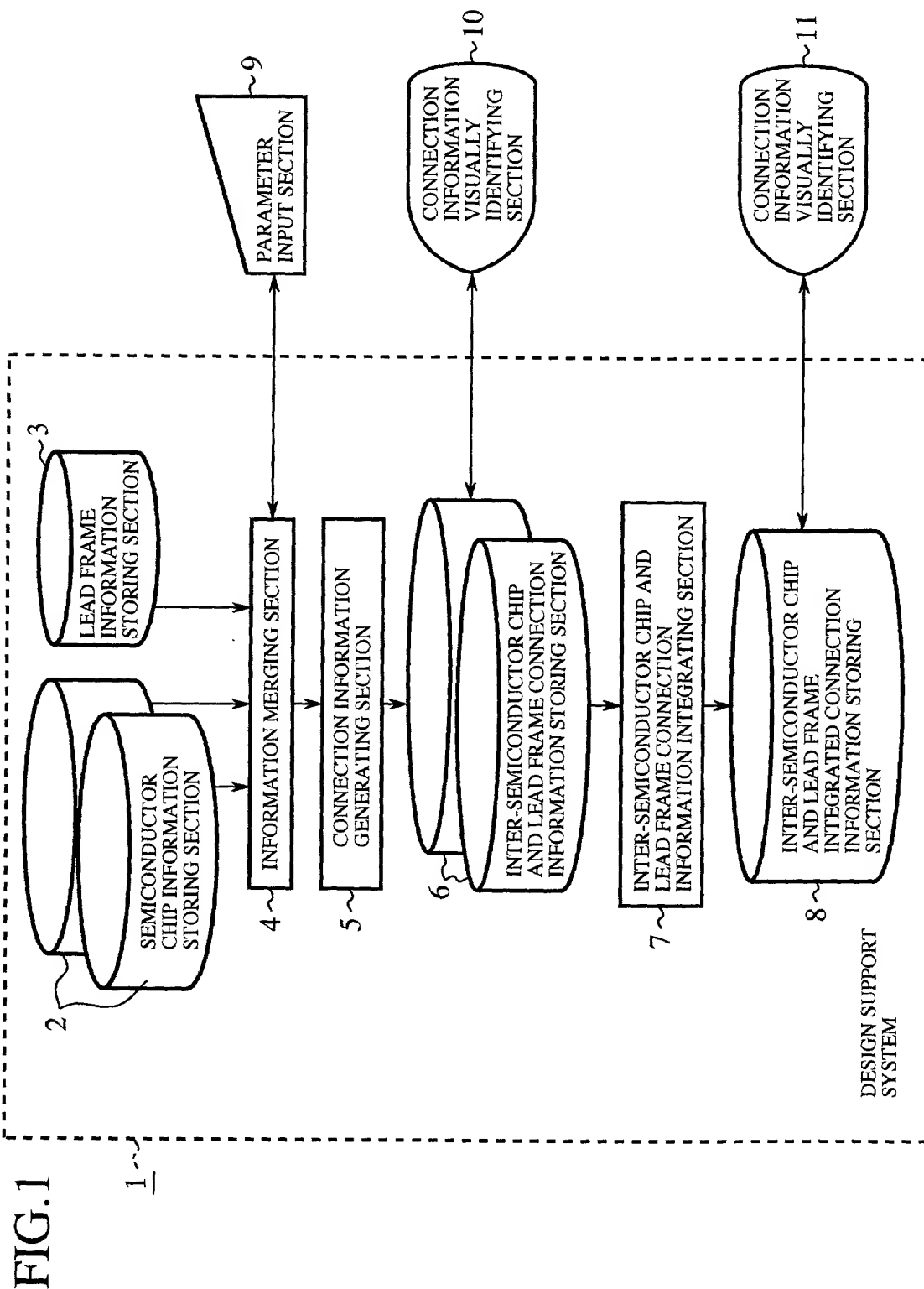


FIG.2

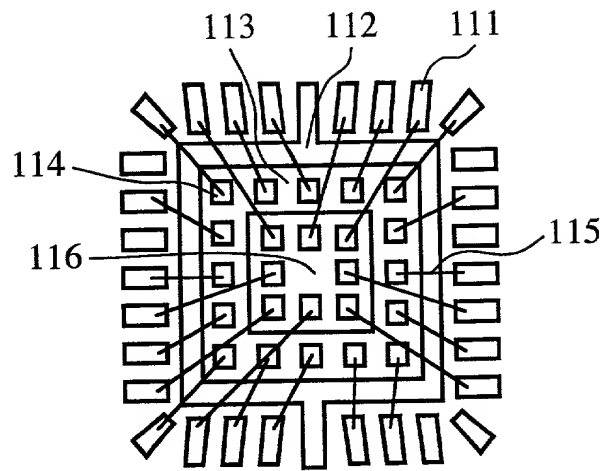


FIG.4

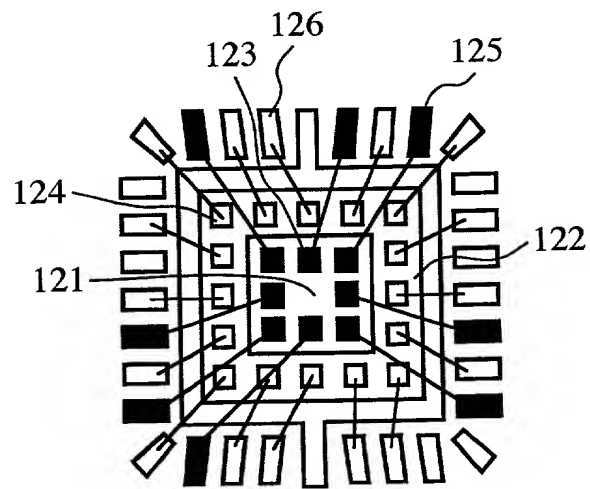


FIG.5

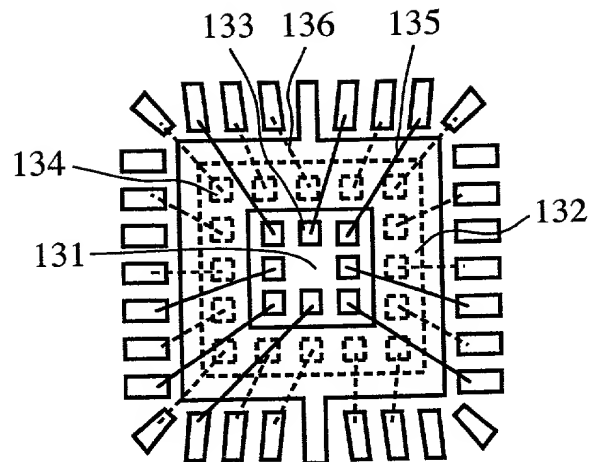


FIG.3

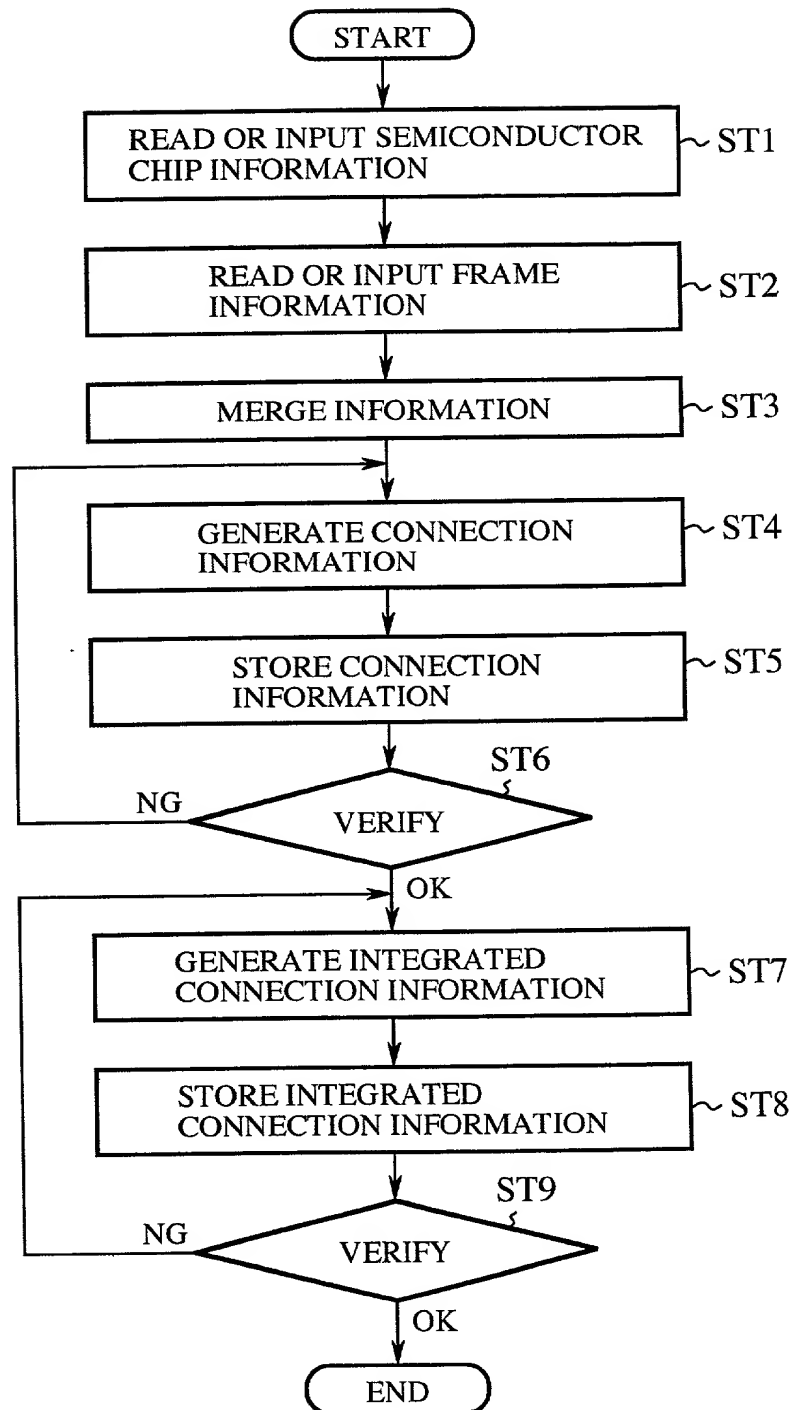


FIG.6

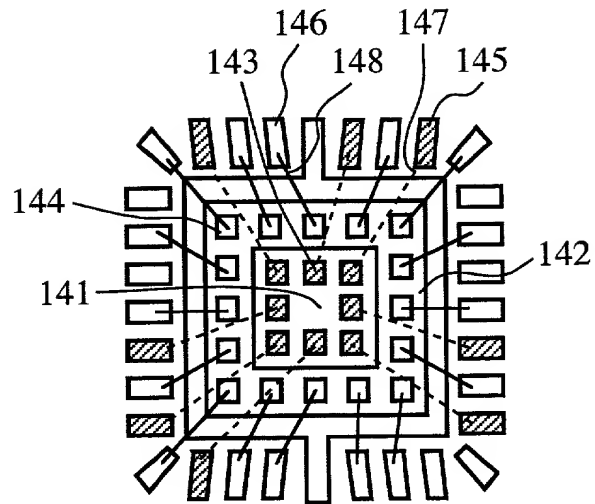


FIG.7

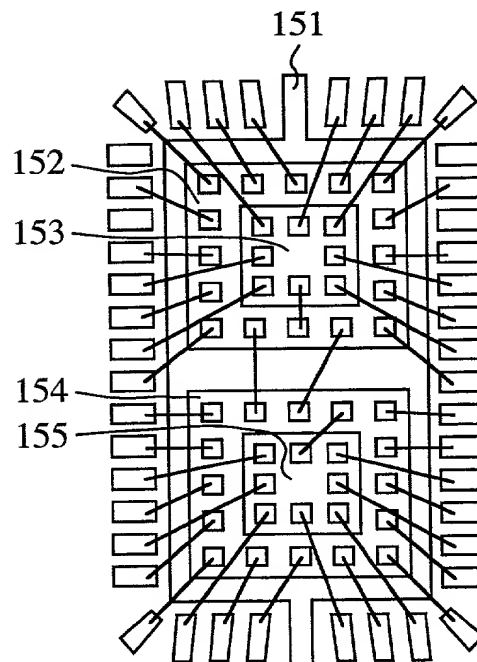


FIG.8

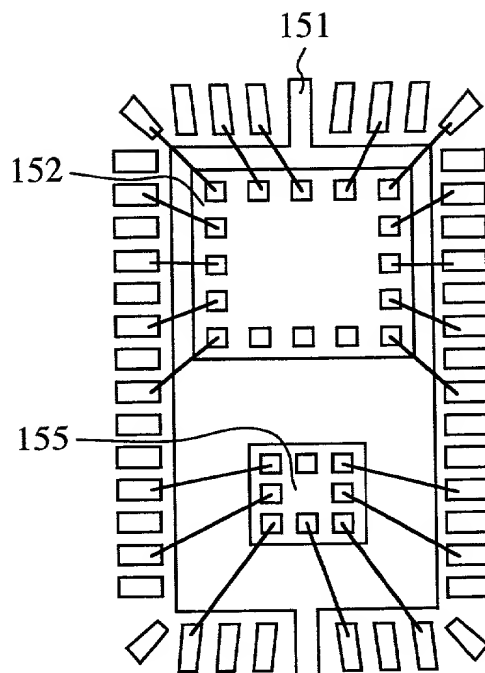


FIG.9

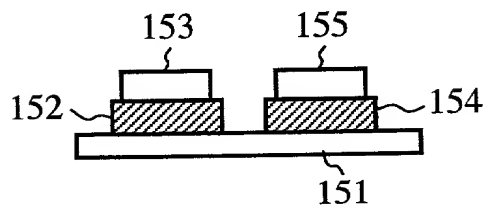


FIG.10

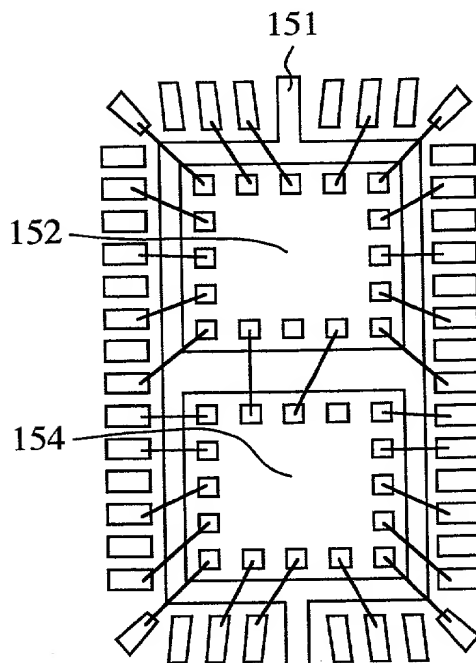


FIG.11

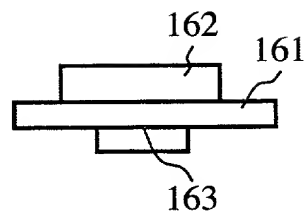


FIG.12

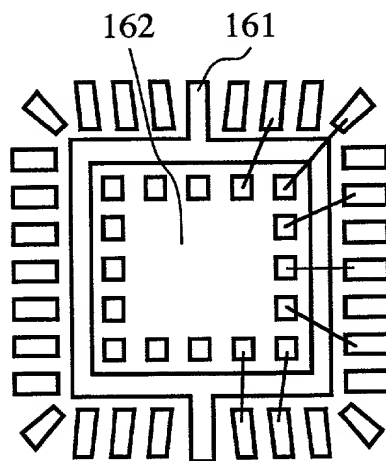


FIG.13

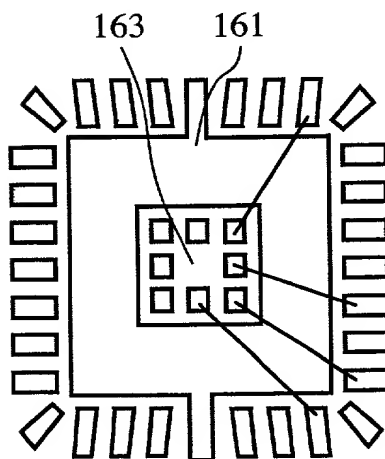


FIG.14

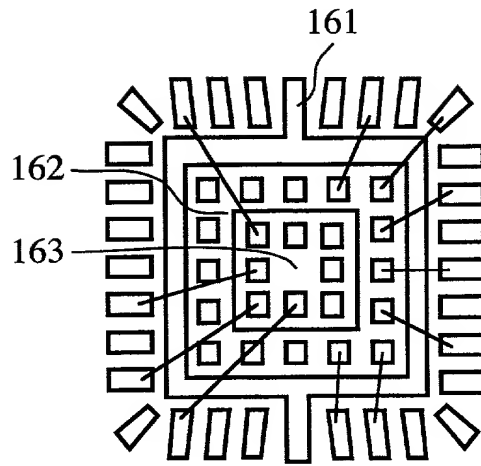


FIG.15

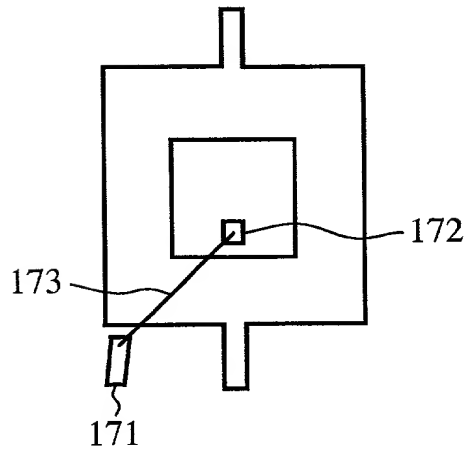


FIG.16

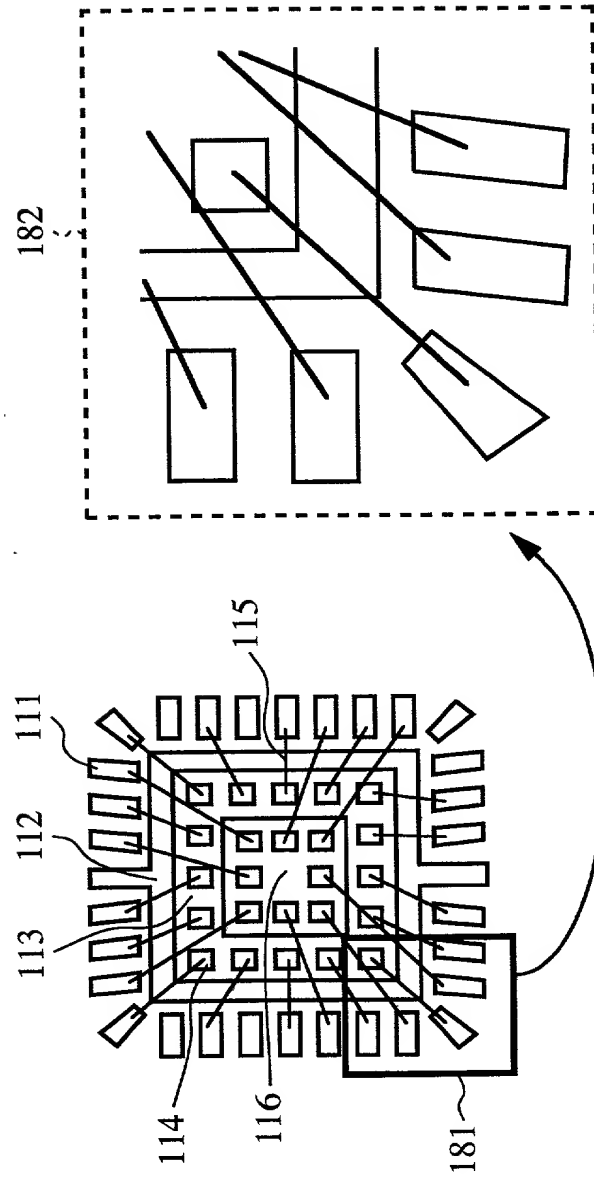


FIG.17

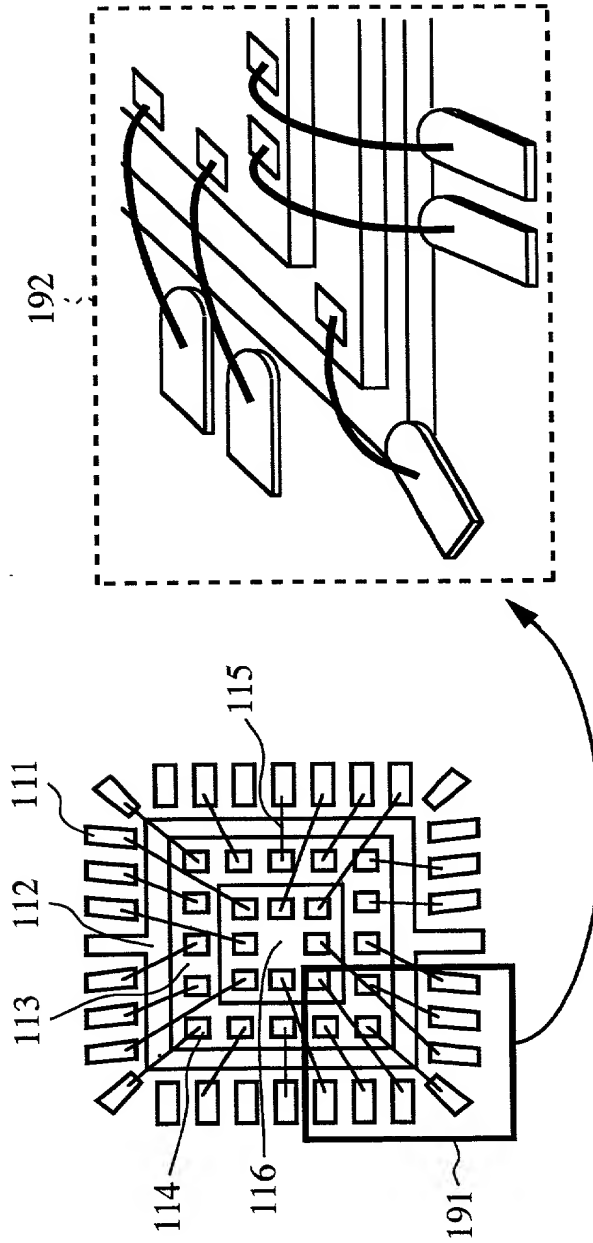


FIG. 18

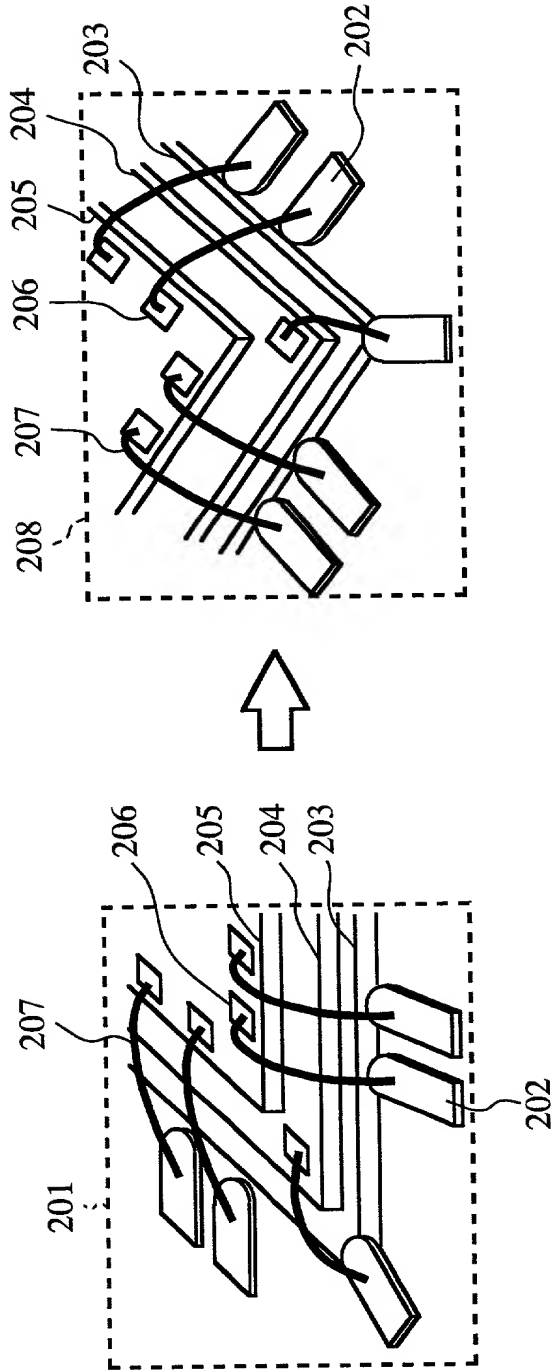


FIG.19

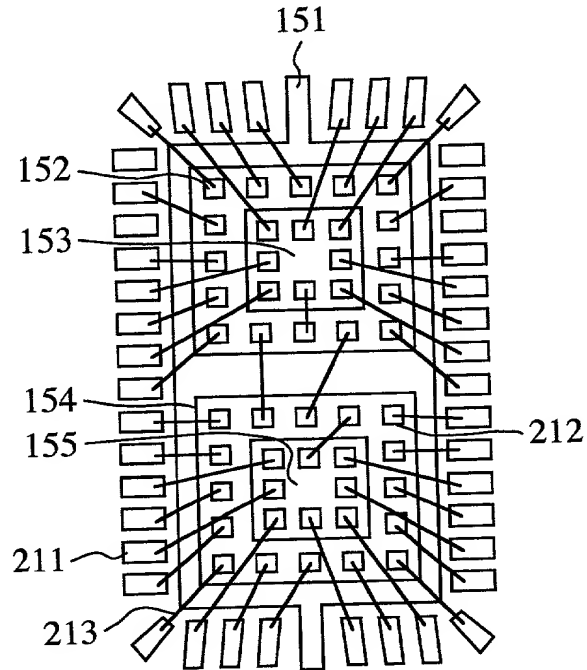


FIG.20

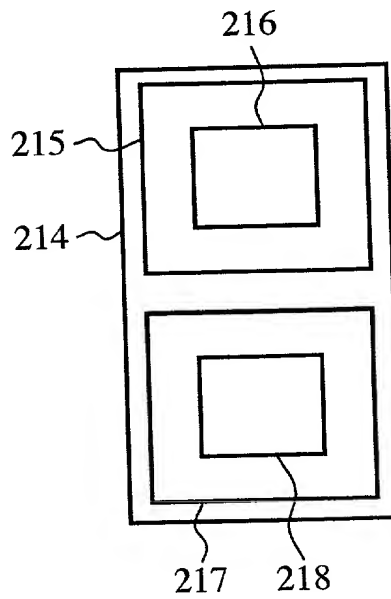


FIG.21

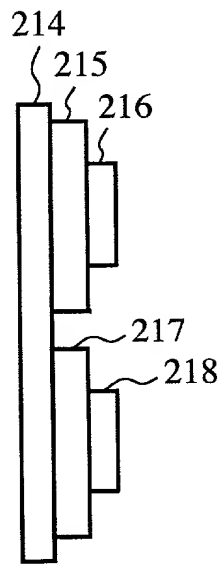


FIG.22

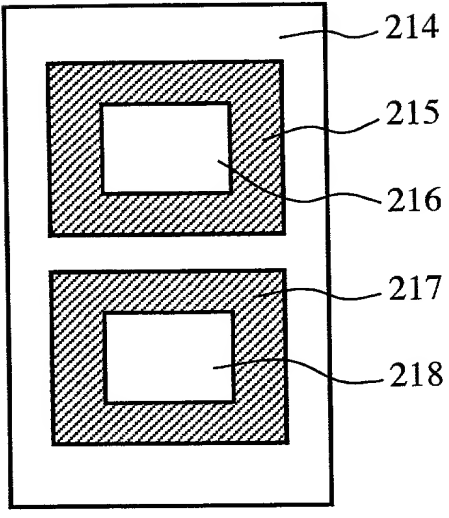


FIG.23

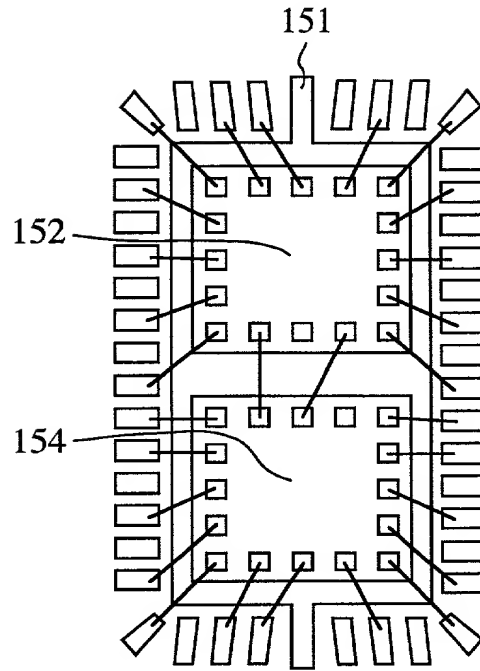


FIG.25

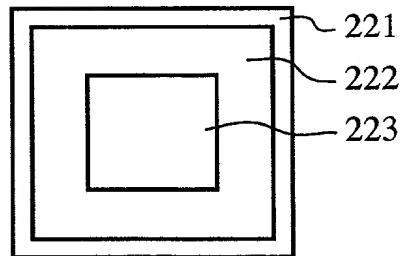


FIG.24

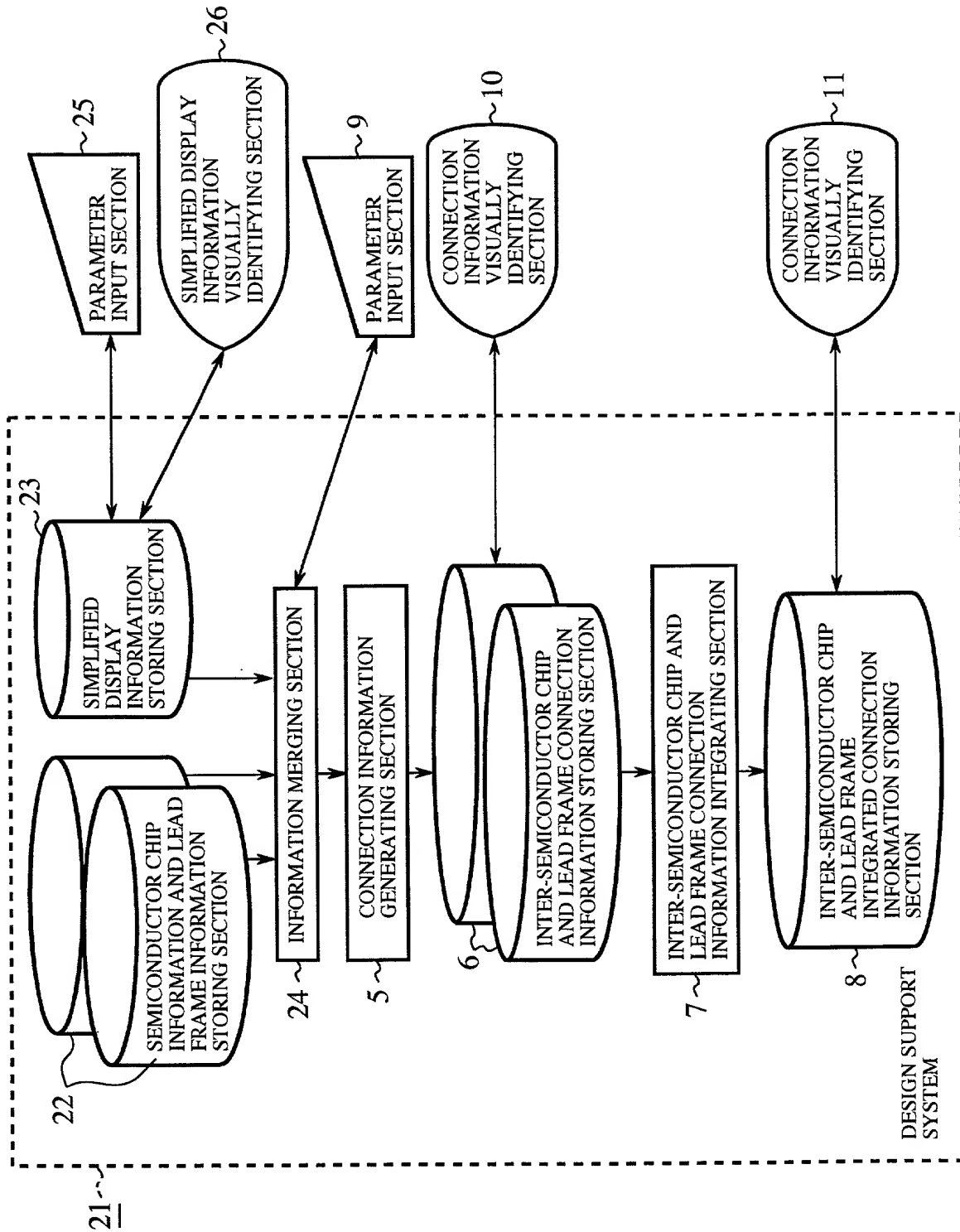


FIG.26

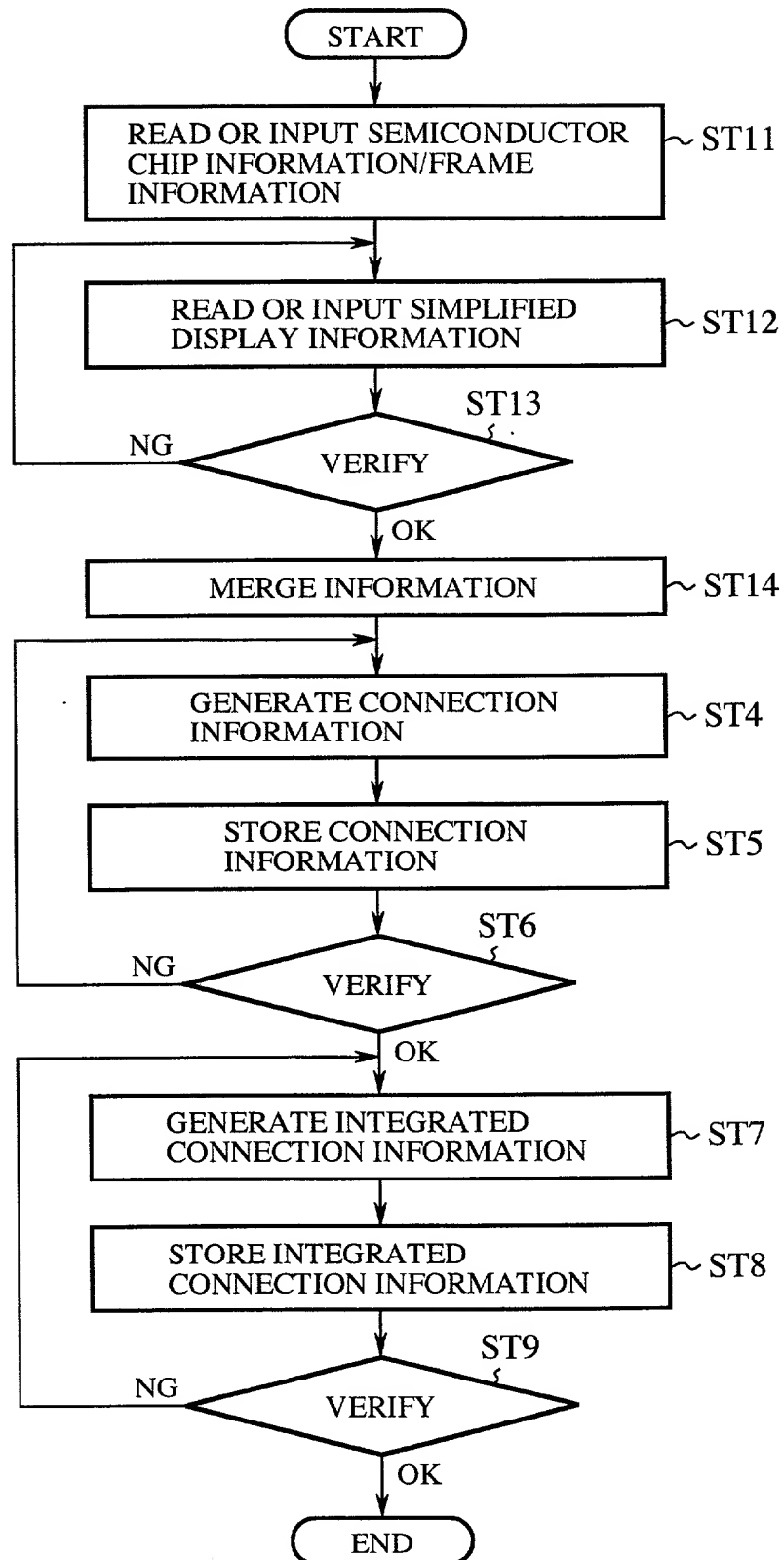


FIG.27

	FRAME	FIRST SEMICONDUCTOR CHIP	SECOND SEMICONDUCTOR CHIP
FRAME	0	16	8
FIRST SEMICONDUCTOR CHIP	16	0	0
SECOND SEMICONDUCTOR CHIP	8	0	0

FIG.28

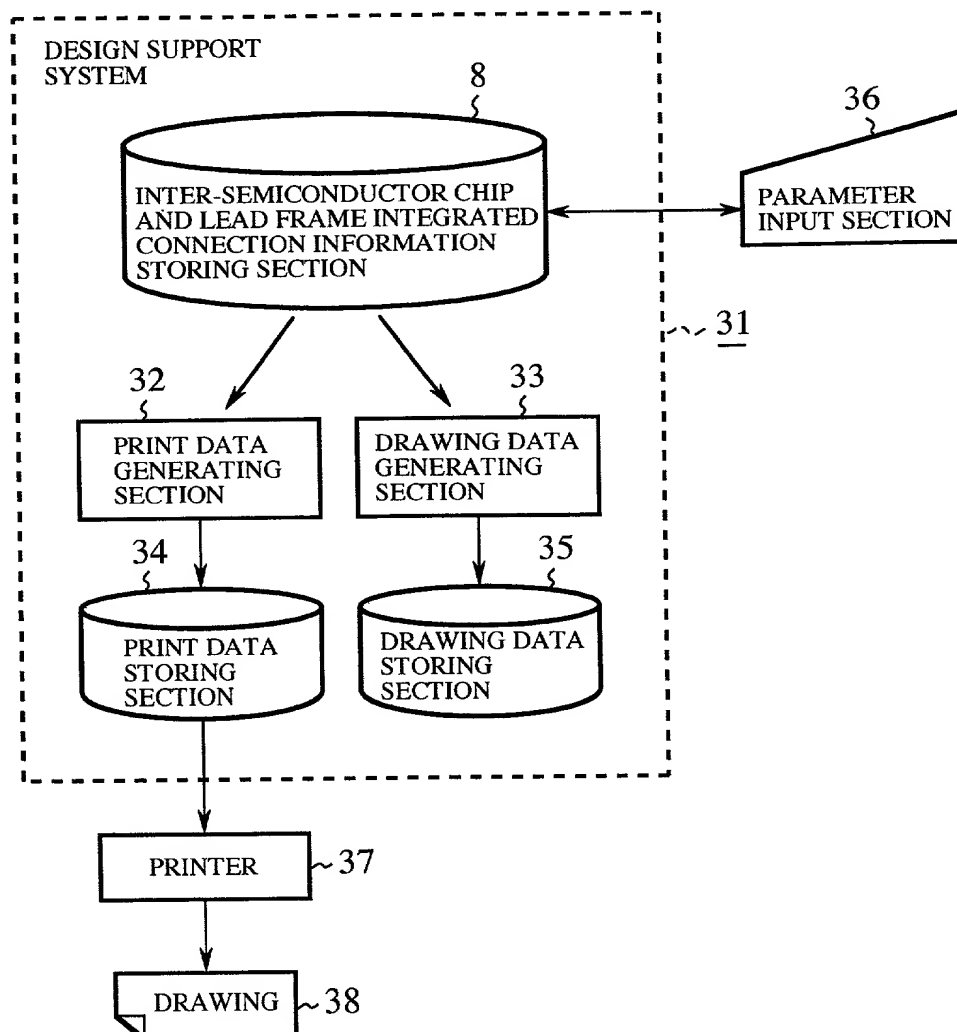


FIG.29

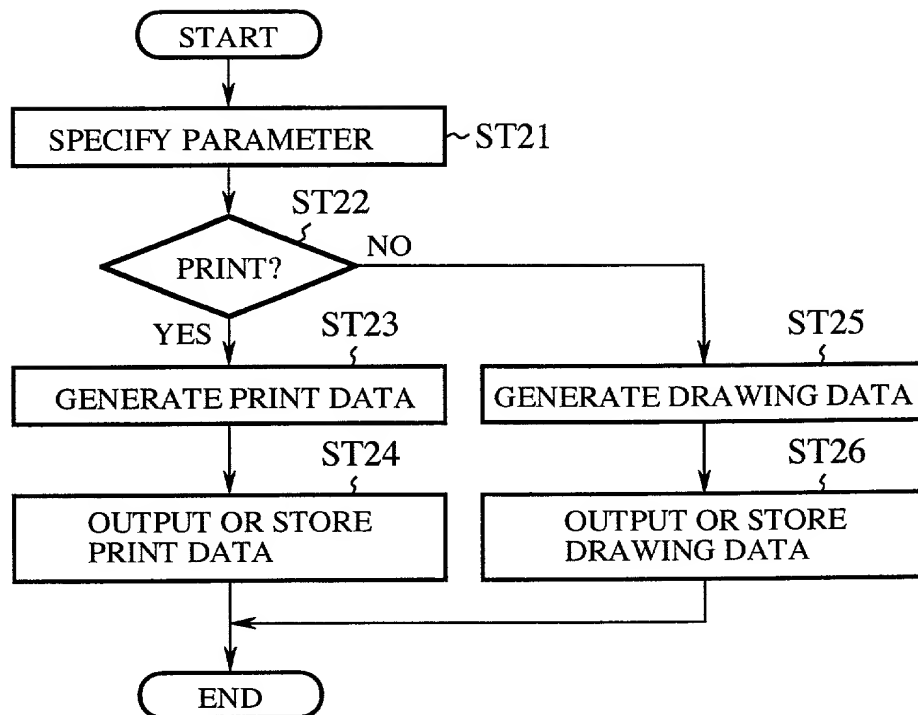
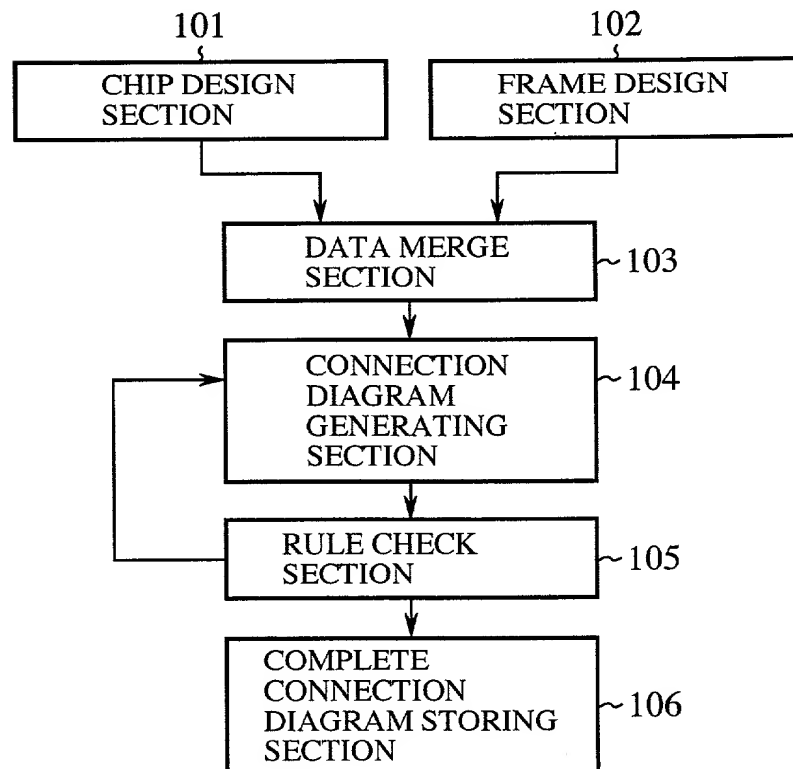
FIG.30
(PRIOR ART)

FIG.31
(PRIOR ART)

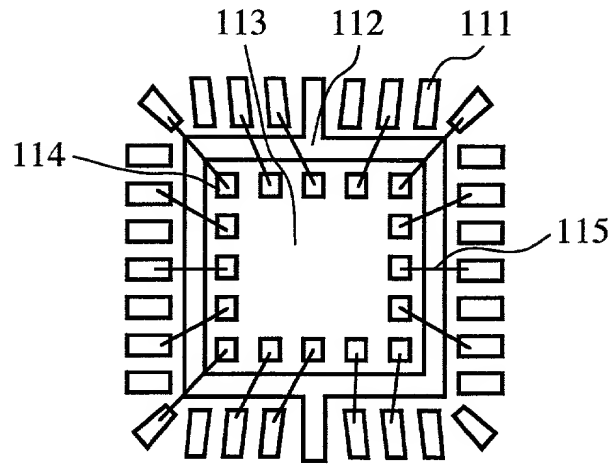


FIG.32
(PRIOR ART)

